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State Key Laboratory of Advanced Displays and Optoelectronics Technologies

香港科技大學
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AND TECHNOLOGY

Hybrid-Phase Metal Oxide Thin-Film Transistor Technology

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Young Leader Conference, ICDT 2021 **2021/06/02**

Outline

Poly-ITO + Poly-ZnO

Element composition

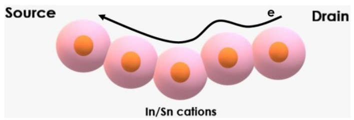
Crystal morphology

Hybrid-phase metal oxide (hp-MO) thin films

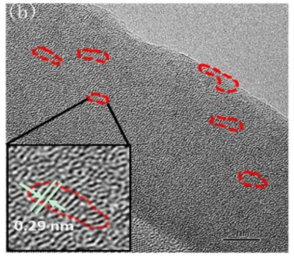
Device & processing innovations

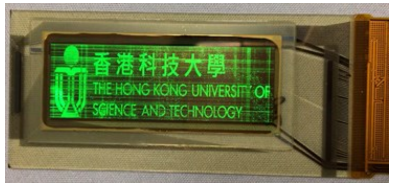
hp-MO thin-film transistors (TFTs)

Practical applications



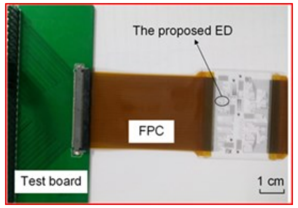
hp-ITZO

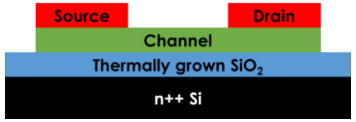




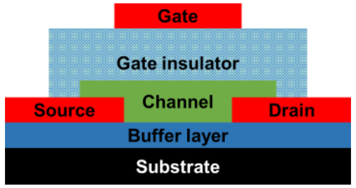
Display panels

Integrated circuits



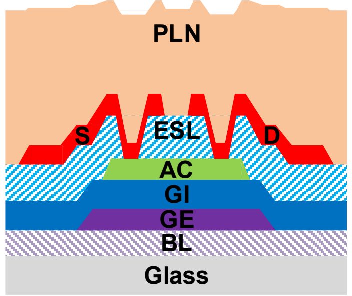


Bottom-gate top-contact (BG-TC)

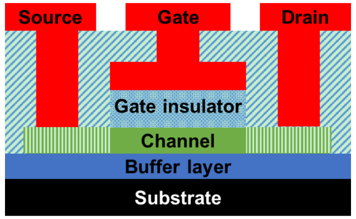


Top-gate Bottom-contact (BG-TC)

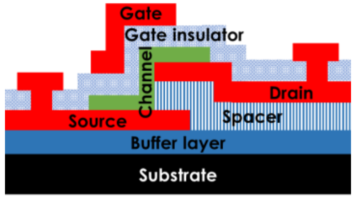
With emphases on their cost-effective manufacturing



Etch-stopper-layer (ESL)



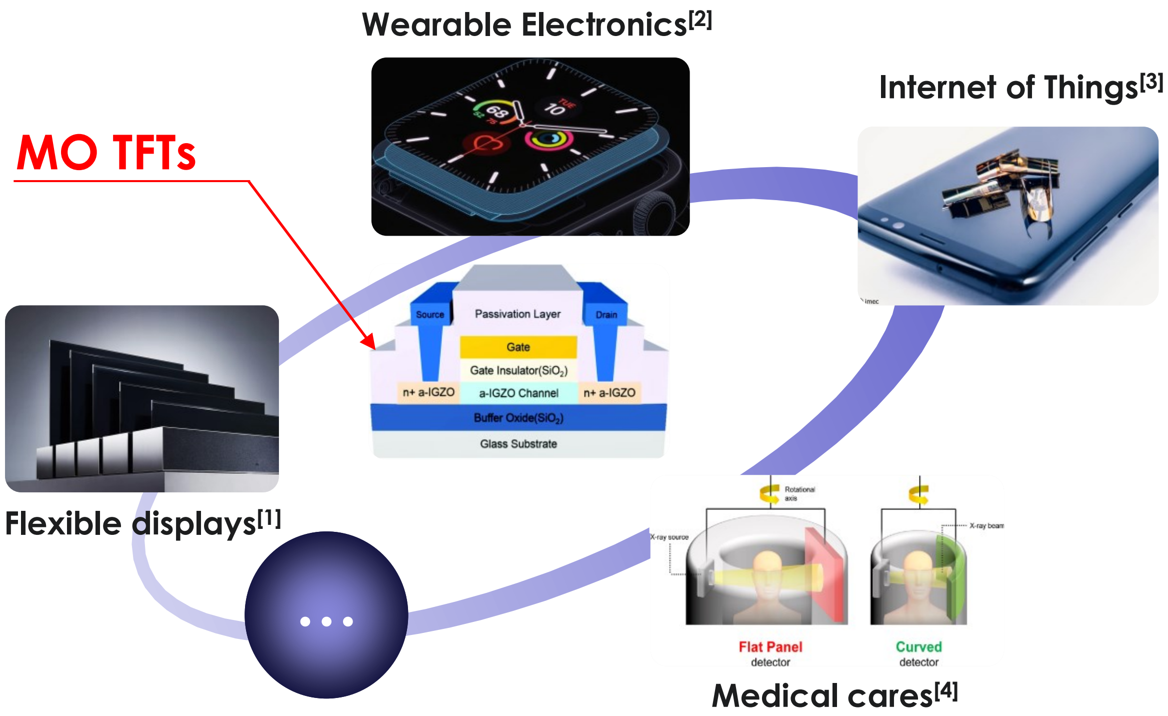
Self-aligned (SA)



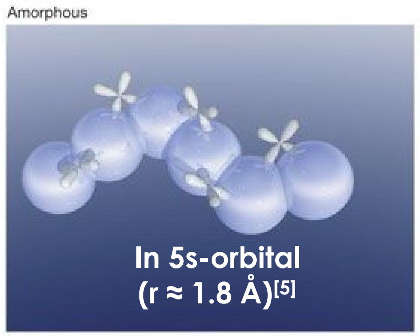
Vertical

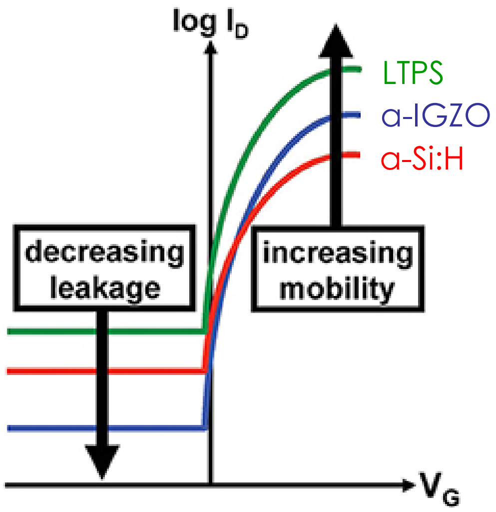
Part 1: hp-ITZO Thin Films

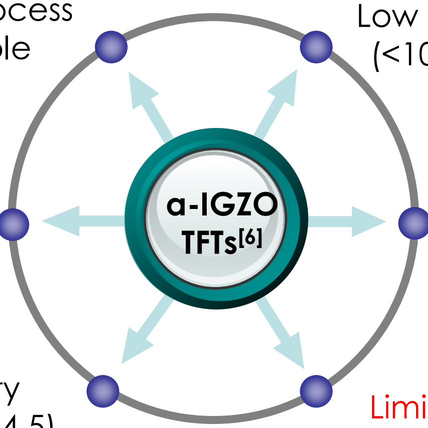
Metal Oxide (MO) TFT Technology



Atomic arrangement of amorphous indium-gallium-zinc oxide (a-IGZO)







a-Si:H TFT process compatible

Low off current ($<10^{-18}$ A/μm)

Low-temp. processing (RT~350 °C)

Steep SS (0.1~0.3 V/dec)

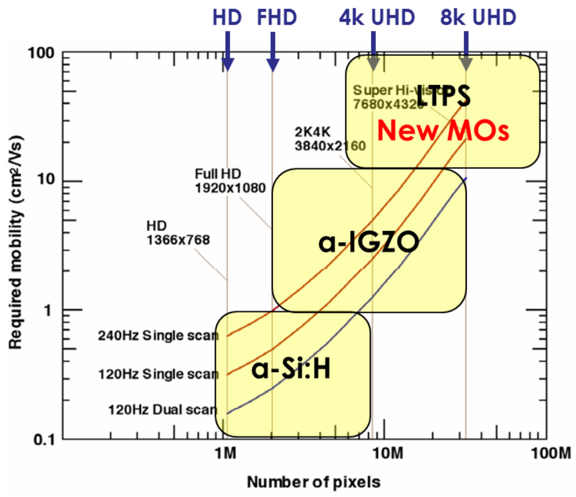
Excellent uniformity (ΔV_{th} < 0.2 V @ Gen 4.5)

Limited mobility (5~10 cm^2/Vs)

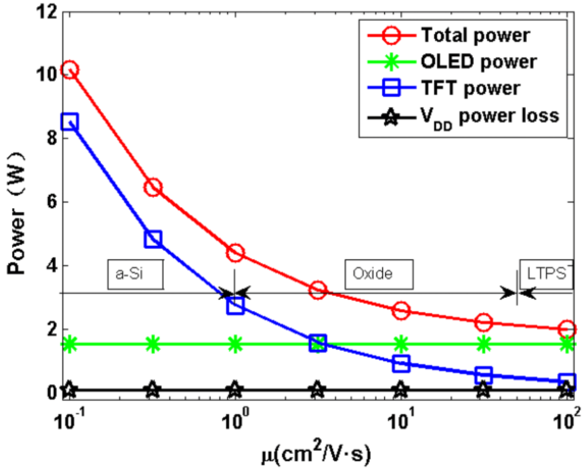
[1] LG Electronics' SIGNATURE website
[2] Apple YouTube Channel
[3] IMEC press release
[4] van Breemen, et al. *npj Flex. Electron.* 4.1 (2020): 1-8.
[5] J. E. Medvedeva, et al. *Adv. Electron. Mater.*, 3(9), 1700082, 2017.
[6] J. F. Wager, *Info. Display*, 32(1), 16-21, 2016..

Call for Higher-Mobility MO TFTs in Displays

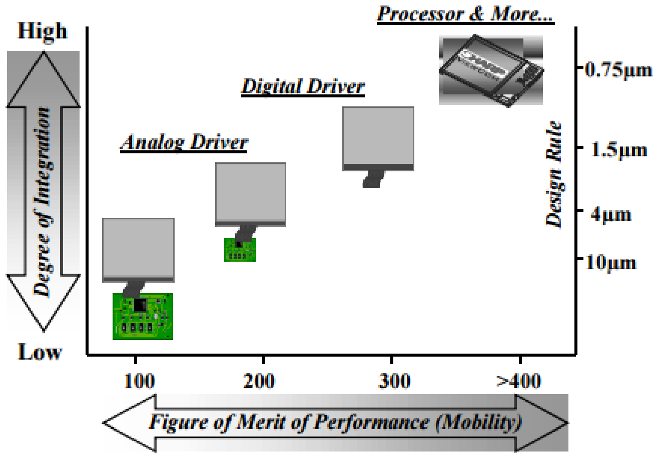
Higher display definitions (resolution, frame rate, size, etc.)[1]



Lower power consumption[2]



System-on-panel integration



$$P_{total} = \sum_{i=R,G,B} (P_{TFT\_i} + P_{OLED\_i}) + P_{Vdd}$$

$$\approx \sum_{i=R,G,B} \frac{L_{subpixel\_i}}{\eta_{OLED\_i}} * A_{subpixel\_i} * \left(\sqrt{\frac{2I_{OLED\_B}}{\mu C_{ox}\frac{W}{L}}} + V_{OLED\_B} \right)$$

$$+ \frac{N^3}{12} \left(\sum_{i=R,G,B} I_{OLED\_i} \right)^2 * \Delta R * M$$

$$I_{dsat} = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_{gs} - V_{th})^2$$

$$t_{sd} = \frac{L^2}{\mu V_{ds}}$$

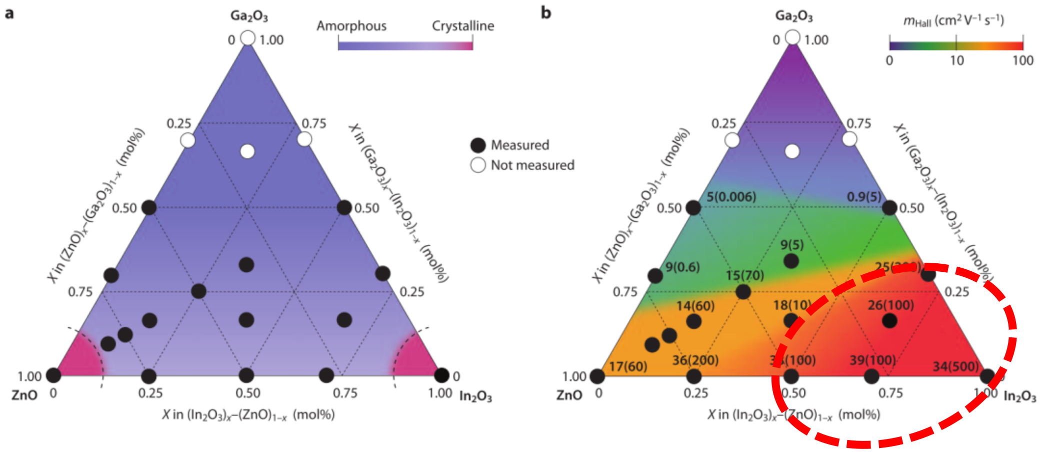
- New low-temperature processed MO semiconductors (beyond a-IGZO) with boosted mobility for large-area electronics?

[1] T. Kamiya, *et al. Sci. Tech. Adv. Mater.*, 11(4), 044305, 2010.
[2] L. Zhou, *et al. J. Display Technol.*, 12(10), 1064-1069, 2016.

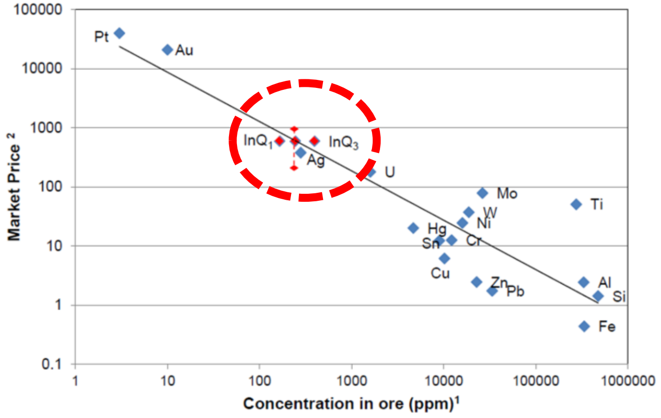
Mobility Boost in AOS Materials

- For common amorphous oxide semiconductor (AOS) materials → element composition modification (e.g., In^{3+} ↑)

In_2O_3-Ga_2O_3-ZnO ternary system[1]



Indium market price[2]



n_{free} ↑ → V_{th} ↓, I_{off} ↑

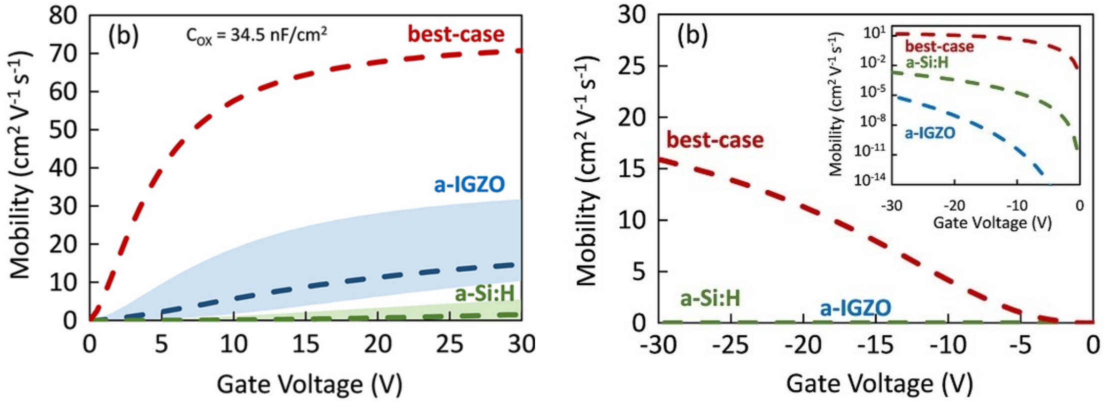
↑

In^{3+} ↑ → μ ↑

↓

cost ↑

However, an upper mobility limit is predicted in AOS.[3,4]



	μ_e (cm^2/Vs)	μ_h (cm^2/Vs)
Typical a-IGZO	≤ 14.7	≤ 8.8×10^{-6}
Best amorphous case	≤ 70.7	≤ 15.9

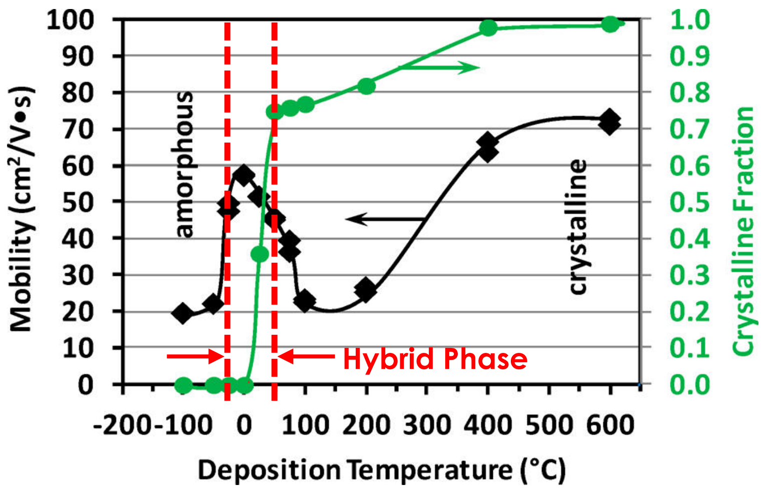
Drude model[5]:

$$\frac{1}{\mu} = \frac{m_e^*}{q}\left(\frac{1}{\tau_{composition}} + \frac{1}{\tau_{crystallinity}} + \frac{1}{\tau_{defect}} + \frac{1}{\tau_{vibron}} + \frac{1}{\tau_{strain}} + \ldots\right)$$

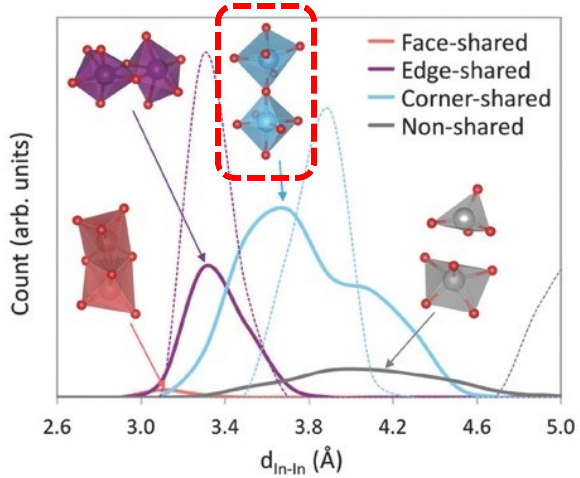
[1] H. Hosono, *J. Non. Cryst. Solids*, 352(9-20), 851-858, 2006.
[2] M. Lokanc, *et al. NREL.*, 2015.
[3] K. A. Stewart, *et al.*, *J. Non. Cryst. Solids*, 432, 196-199, 2016.
[4] K. A. Stewart, *et al. J. Soc. Info. Display*, 24(6), 386-393, 2016.
[5] J. E. Medvedeva, *et al. Adv. Electron. Mater.*, 3(9), 1700082, 2017.

Hall Mobility vs. Crystallinity in In_2O_3 Films

Hall mobility of In_2O_3 film with different crystallinities



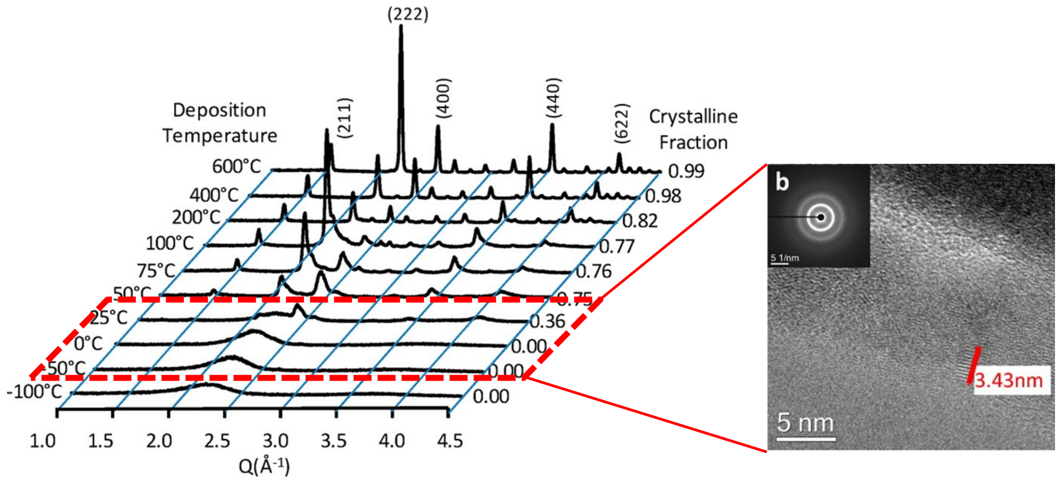
InO polyhedra interconnection in In_2O_3 films with low (solid) and high (dashed) crystallinity



InO_x inter-connection	Ave. In-In distance	Ave. In-O-In angle	Remark
Non-shared	3.8 Å	-	In 5s-orbital radius ≈ 1.8 Å
Corner-shared	3.5 Å	115°	
Edge-shared	3.3 Å	98°	
Face-shared	3.1 Å	71°	

Best spatial extension capability for overlapped indium 5s-orbitals.

XRD spectra and HRTEM image of hp-In_2O_3 films



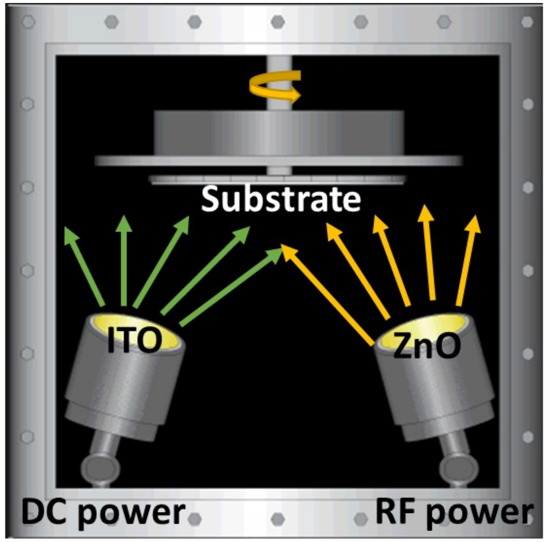
- ✓ Hybrid phase (hp): the onset of crystallization (>80% InO_x polyhedra are corner-shared)
- → Efficient long-distance chaining for the formation of well-defined electron percolation conduction paths
- → Hall mobility peak, good electrical uniformity, low-temperature processing, etc.

- ❑ Binary hp-In_2O_3 → Multicomponent hp-MO for cost reduction ?

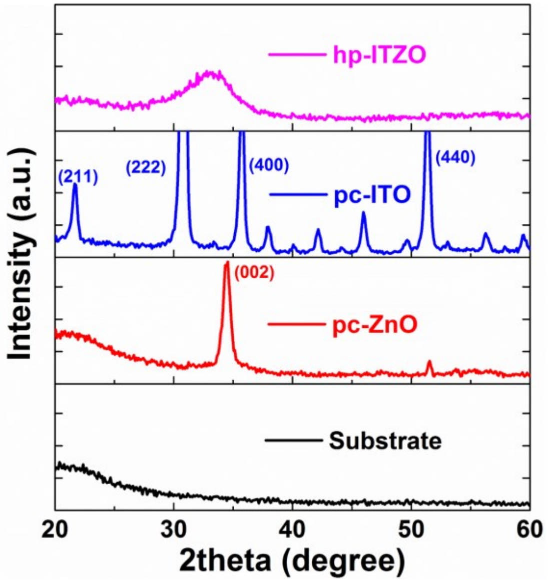
[1] D.B. Buchholz, *et al. Chem. Mater.*, 26(18), 5401-5411, 2014.
[2] J. E. Medvedeva, *et al. Adv. Electron. Mater.*, 3(9), 1700082, 2017.

hp-ITZO Thin Film Deposition

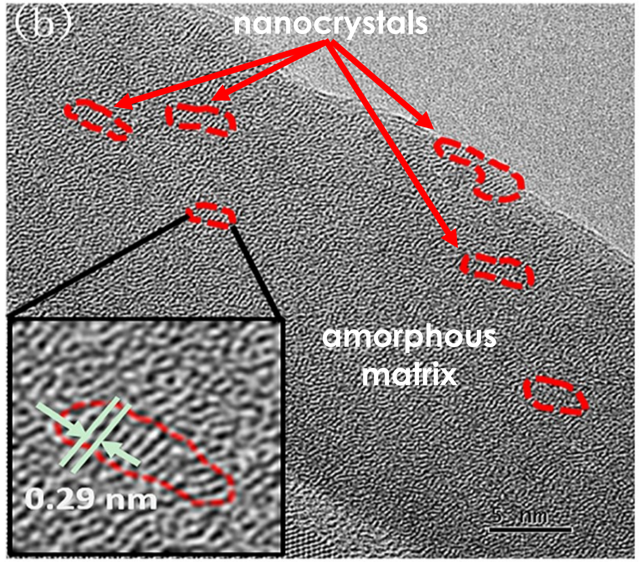
Poly-ITO + Poly-ZnO



hp-ITZO



XRD spectra

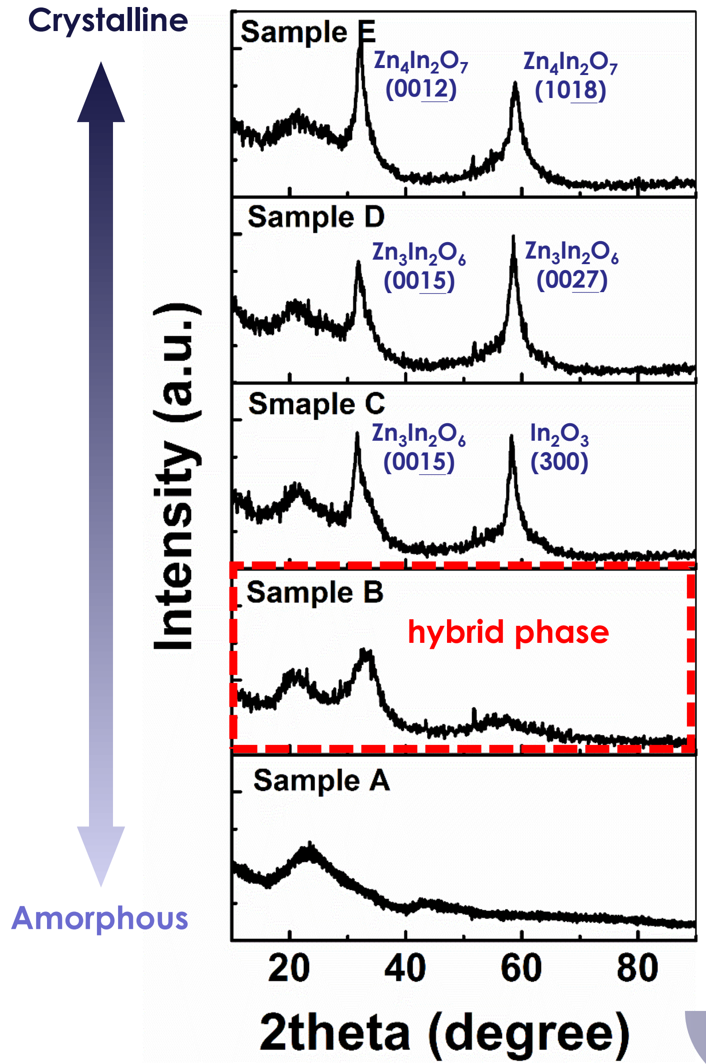


HRTEM image

- ✓ hp-ITZO thin films: an amorphous matrix with a number of columnar nanocrystals (including ZnO, $Zn_3In_2O_6$, $Zn_4In_2O_7$, etc.) embedded.
- ❑ Similar XRD spectrum and HRTEM image → Hall mobility peak?

S. Deng, *et al. Appl. Phys. Lett.*, 109(18), 182105, 2016.
S. Deng, *et al. IEEE Trans. Electron Devices*, 64(8), 3174-3182, 2017.
Best Oral Presentation Award, 2016 PG workshop on Display Research.

Hall Mobility vs. Crystallinity in ITZO Thin Films



AOS upper mobility limit estimation model[1]

$$\mu^{-1} = \mu_{drift}^{-1} + \mu_{diff}^{-1}$$

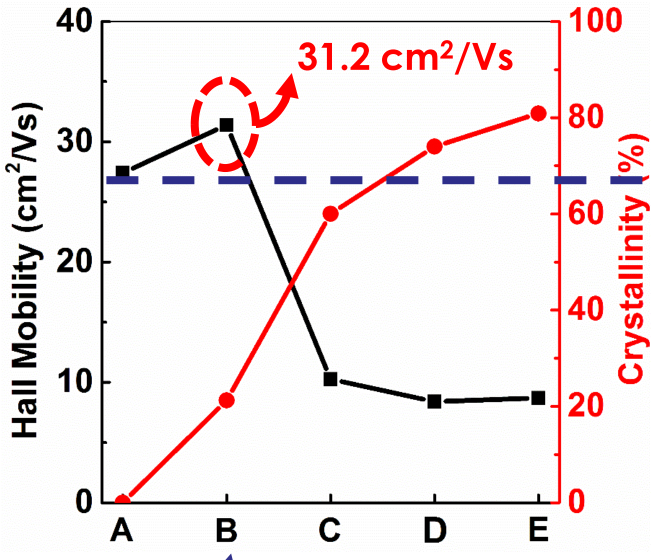
$$\mu_{drift} = \frac{n}{n+n_T}\mu_0 = \frac{n}{n+n_T}\cdot\frac{q\hbar}{6m_e^* k_B T}$$

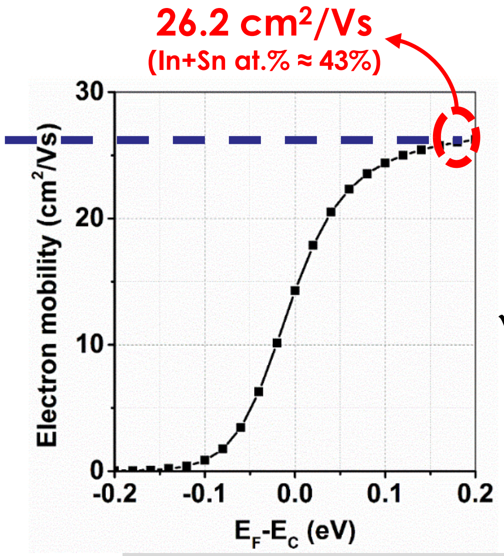
$$\mu_{diff} = \mu_{drift}\frac{n}{N_C} = \mu_{drift}\frac{n}{2\left(\frac{2\pi m_e^* k_B T}{h^2}\right)^{\frac{3}{2}}}$$

$$n = \int_{E_C}^{\infty} g_C(E)f(E)dE = \int_{E_C}^{\infty}\left[n_{TA} + \frac{1}{2\pi^2}\left(\frac{2m_e^*}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E-E_C}\right]f(E)dE$$

$$n_T = \int_{E_V}^{E_C} g_{TA}(E)f(E)dE = \int_{E_V}^{E_C} n_{TA}\exp\left(\frac{E-E_C}{E_U}\right)f(E)dE$$

m_e^* - effective mass of electron
E_U - Urbach energy (related to tail states)
n_{TA} - peak density of conduction band tail states

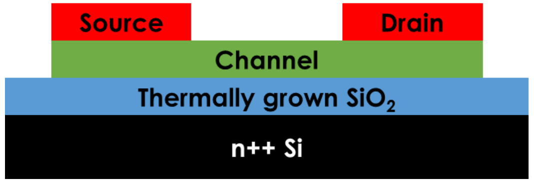




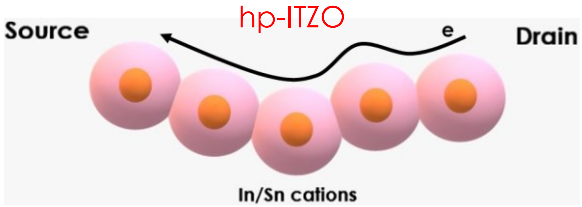
- ✓ hp-ITZO can surpass the upper mobility limit in its amorphous counterpart.

[1] K. A. Stewart, *et al.*, *J. Non. Cryst. Solids*, 432, 196-199, 2016.

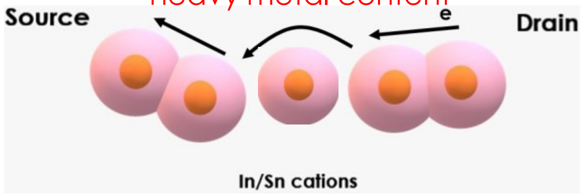
Field-Effect Mobility in hp-ITZO Channels



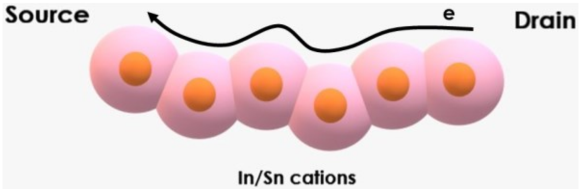
hp-ITZO

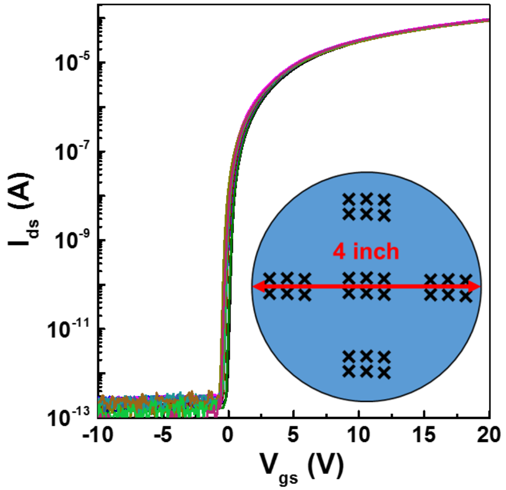


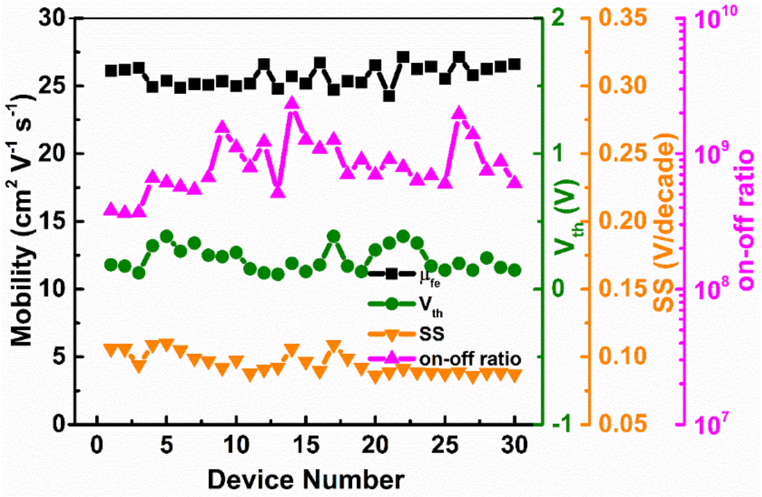
a-ITZO with insufficient heavy metal content



a-ITZO with excess heavy metal cations







Comparison of hp-ITZO with other representative MO channels

Channel	(In+Sn)/(In+Sn+Zn) at. %	μ_{fe} (cm^2/Vs)	On-off ratio
a-ITZO [1]	>66.7	27.9	1.1×10^8
CAAC-ITZO [2]	>66.7	20.2	$\sim10^{16}$
a-IGZO [3]	>33.4	10.1	$>10^9$
CAAC-IGZO [4]	>33.4	7.7	$\sim10^{19}$
Poly-ZnO [5]	0	12	$\sim10^8$
a-ITO [6]	100	29	$\sim10^8$
hp-ITZO [7]	41.3	27.3	$>10^9$

*hp-ITZO = ITO-stabilized ZnO

✓ The utilization of corner-shared InO_x polyhedra rather than the increase of In content for mobility boost.

→ Cost-effective TFT channels

[1] T. M. Pan, et al. *IEEE Trans. Electron Devices*, 64(5), 2233-2238, 2017.

[2] T. Takasu, et al. J. Soc. Info. Disp., 23(12), 593-599, 2015.

[3] K. Nomura, et al. *Appl. Phys. Lett.*, 95(1), 013502, 2009.

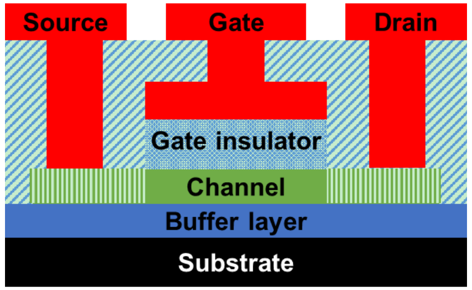
[4] S. Yamazaki, et al. *Jpn. J. Appl. Phys.*, 53(4S), 04ED18, 2014.

[5] H. U. Li, et al. *IEEE Electron Device Lett.*, 36(1), 35-37, 2014.

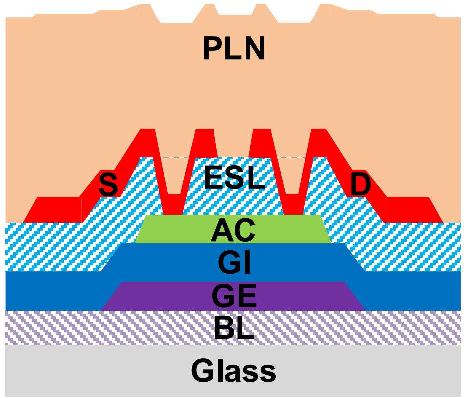
[6] Y. Shao, et al. *Adv. Func. Mater.*, 24(26), 4170-4175, 2014.

[7] S. Deng, *et al. IEEE Trans. Electron Devices*, 64(8), 3174-3182, 2017.

Part 2: (Cost-Effective) hp-ITZO TFTs

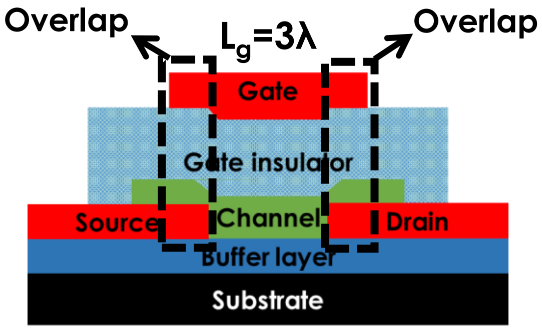


Self-aligned (SA) TFT

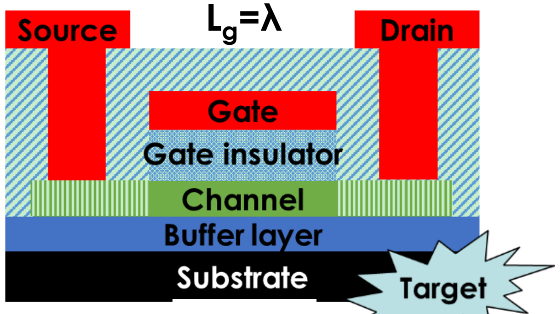


Etch-stopper-layer (ESL) TFT

SA hp-ITZO TFTs (I)

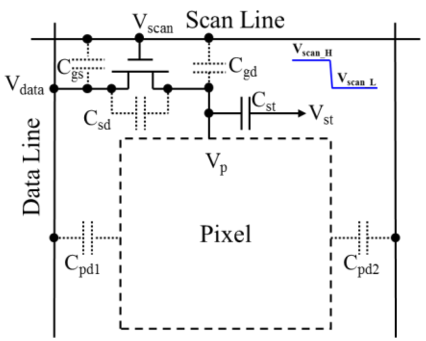


TG-BC TFTs



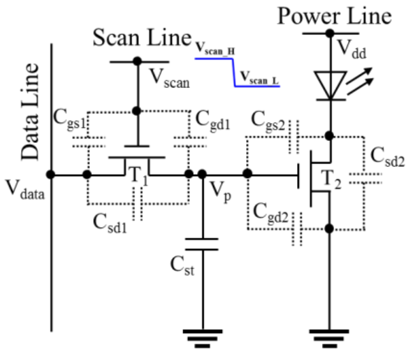
SA TFTs

AMLCD 1T1C circuit



$$\Delta V_p = \frac{C_{gd}\Delta V_{scan} + C_{sd}\Delta V_{data}}{C_{gd} + C_{st} + C_{LC} + C_{sd}} \cong \frac{C_{gd}\Delta V_{scan}}{C_{gd} + C_{st} + C_{LC} + C_{sd}}$$

AMOLED 2T1C circuit



$$\Delta V_p = \frac{C_{gd1}\Delta V_{scan} + C_{sd1}\Delta V_{data} + C_{gs2}\Delta V_{OLED}}{C_{gd1} + C_{sd1} + C_{st} + C_{gs2} + C_{gd2}} \cong \frac{C_{gd1}\Delta V_{scan} + C_{gs2}\Delta V_{OLED}}{C_{gd1} + C_{sd1} + C_{st} + C_{gs2} + C_{gd2}}$$

ΔV_p = kickback/feedthrough voltage

Advantages:

- ✓ Minimized parasitic capacitance → RC delay ↓ & ΔV_p ↓ → accurate signal control
- ✓ Strong device scalability → higher-resolution displays
- ✓ One photolithography step removal → cost-effective manufacturing
- ✓ … …

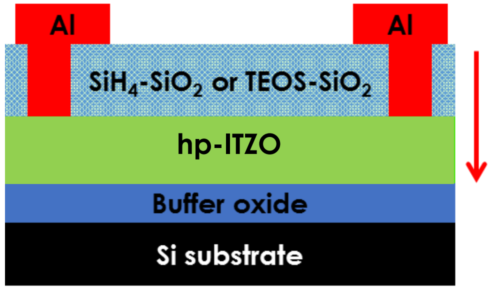
Key issue:

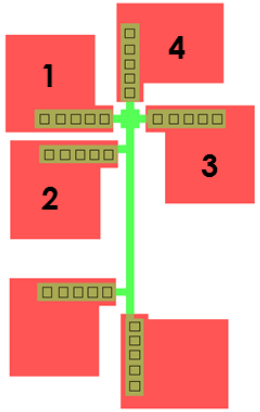
- ❑ Formation of highly conductive & thermally reliable S/D regions (e.g., plasma treatment? Ion doping?)
- → Two different PECVD SiO_2 capping layers + differentiated O_2 annealing strategy

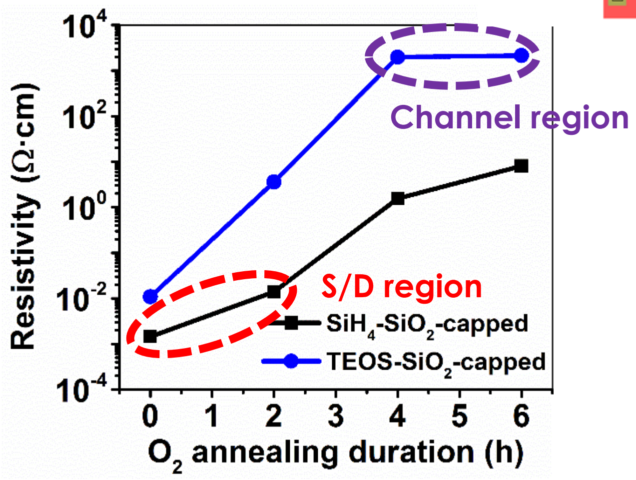
S. Deng, et al. *IEEE Electron Devices Lett.*, 38(12), 1676-1679, 2017.
Distinguished Poster Award, IDMC'17.

SA hp-ITZO TFTs (II)

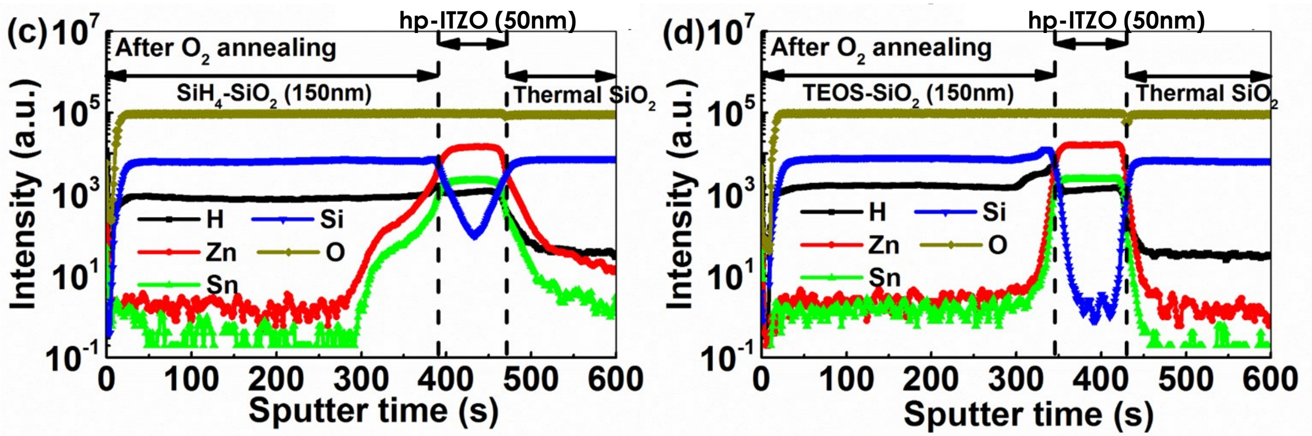
- **How to form conductive & stable S/D region?**







Si depth profile in hp-ITZO with difference capping layers



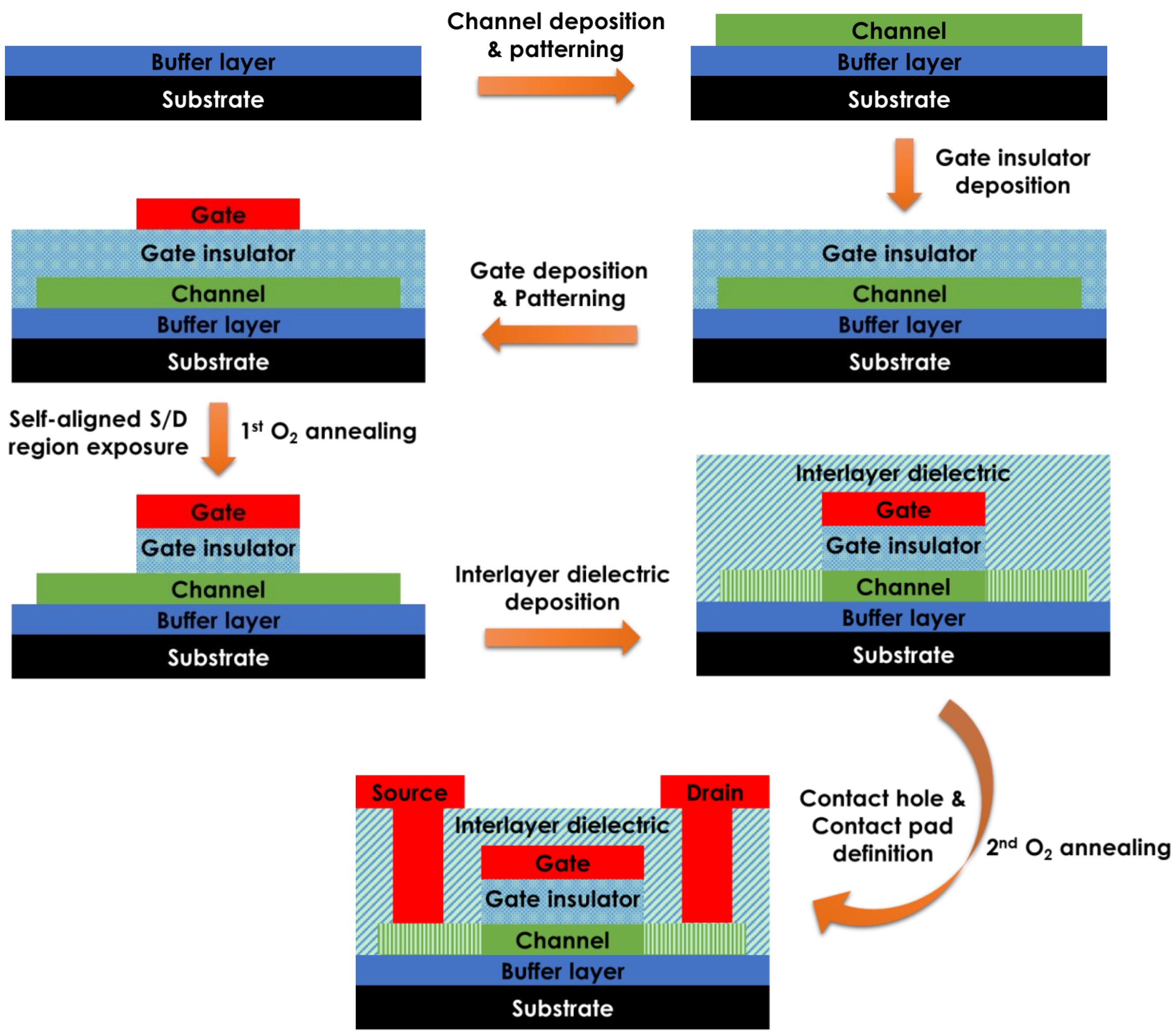
- ✓ Capped by TEOS-SiO_2 → high-resistivity state → intrinsic channel regions
- ✓ Capped by SiH_4-SiO_2 → low-resistivity state (caused by unexpected donor-like Si doping during the deposition of SiH_4-SiO_2) → conductive S/D regions

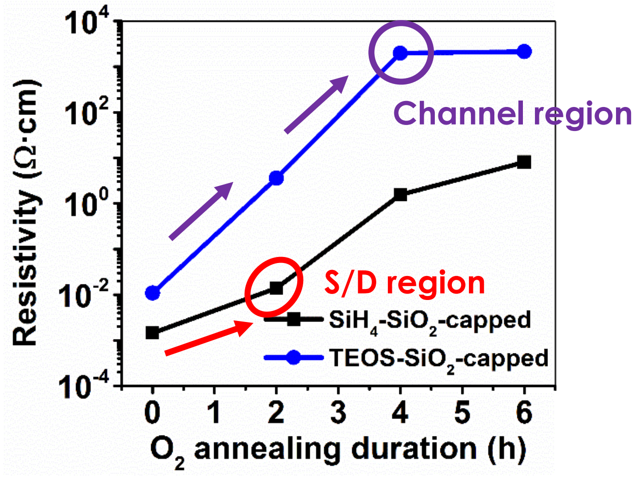
SiH_4-SiO_2 = silane-sourced PECVD SiO_2
TEOS-SiO_2 = tetraethyl-orthosilicate-sourced PECVD SiO_2

S. Deng, et al. *IEEE Electron Devices Lett.*, 38(12), 1676-1679, 2017.
Distinguished Poster Award, IDMC'17.

SA hp-ITZO TFTs (III)

- **Process flow**



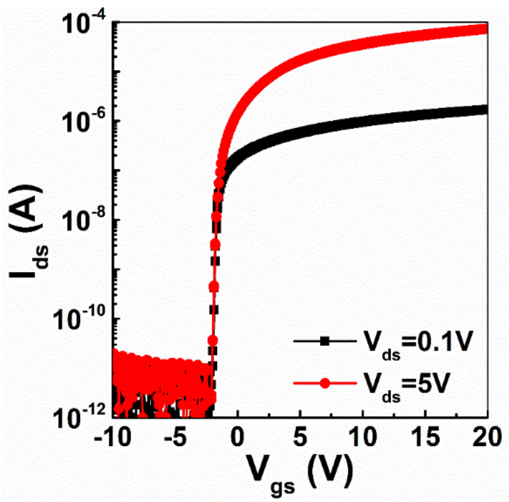


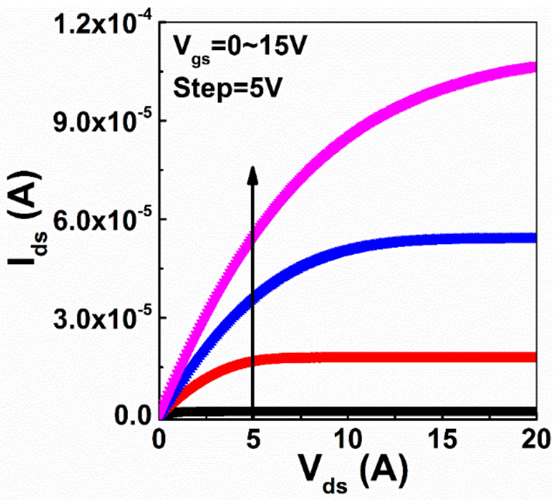
- Gate insulator: TEOS-SiO_2
- 1st O_2 annealing at 300 ˚C for 2 h
- Interlayer dielectric: SiH_4-SiO_2
- 2nd O_2 annealing at 300 ˚C for 2 h

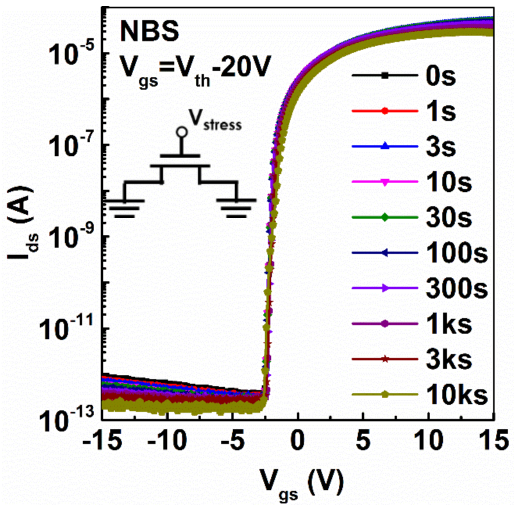
✓ The upper temperature limit of the whole processes is 300 ˚C.

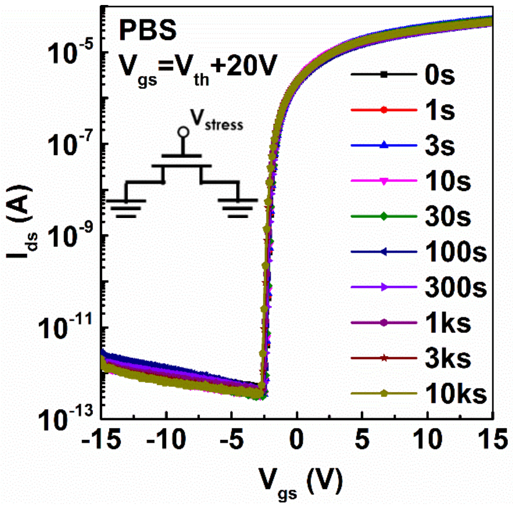
S. Deng, et al. *IEEE Electron Devices Lett.*, 38(12), 1676-1679, 2017.
Distinguished Poster Award, IDMC'17.

SA hp-ITZO TFTs (IV)



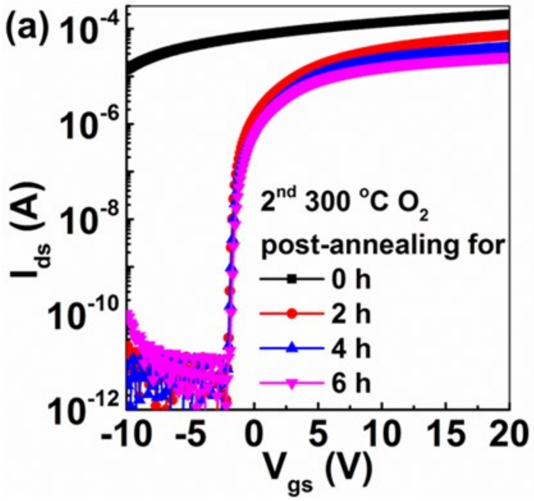






Summary of key electrical parameters

μ_{fe} (cm^2/Vs)	V_{th} (V)	On-off ratio	SS (V/dec)	$\lvert\Delta V_{th}\rvert$ after 10 ks PBS (V)	$\lvert\Delta V_{th}\rvert$ after 10 ks NBS (V)
19.56	-1.65	~10^8	0.105	-0.2	-0.35



- ✓ Thermally stable S/D regions
- → Extremely steep SS & excellent device stability against gate-bias stress

S. Deng, et al. *IEEE Electron Devices Lett.*, 38(12), 1676-1679, 2017.
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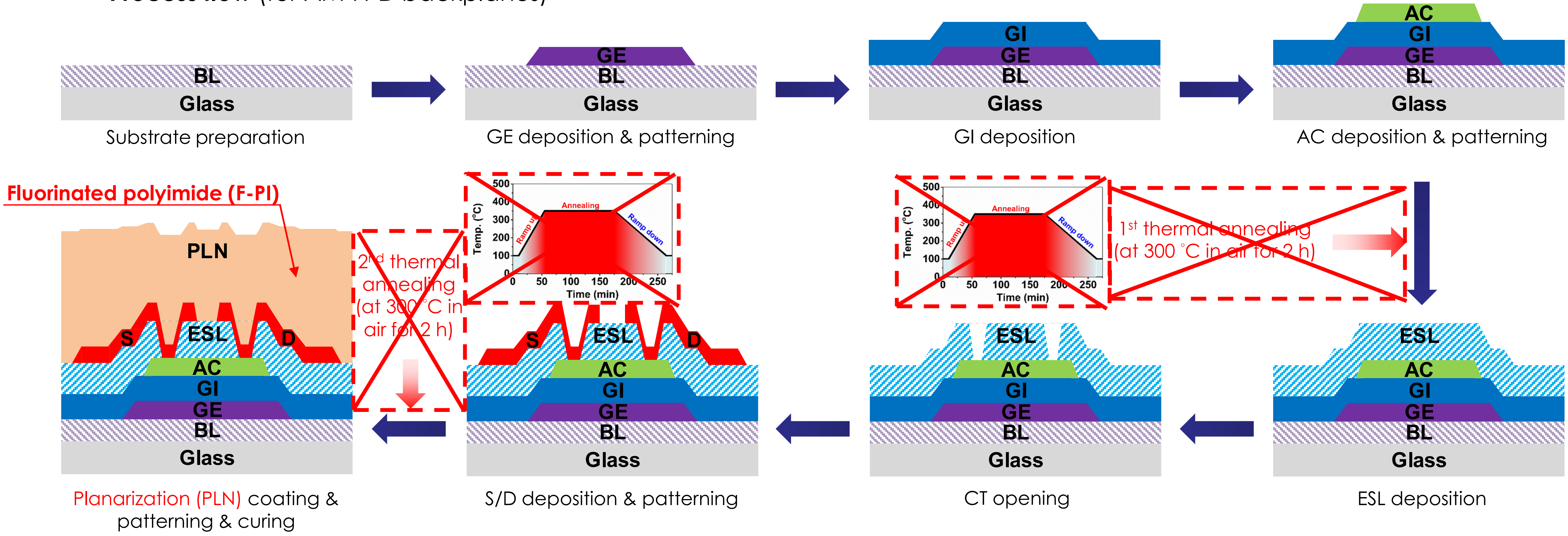
ESL hp-ITZO TFTs (I)

- **Process flow** (for AM-FPD backplanes)



… …

- Simplified process flow (w/o 1st & 2nd thermal annealing) → Device F0
- General process flow (w/ 1st & 2nd thermal annealing) → Device F1

S. Deng, et al. *J. Soc. Info. Disp.* 29, 318-327, 2021.
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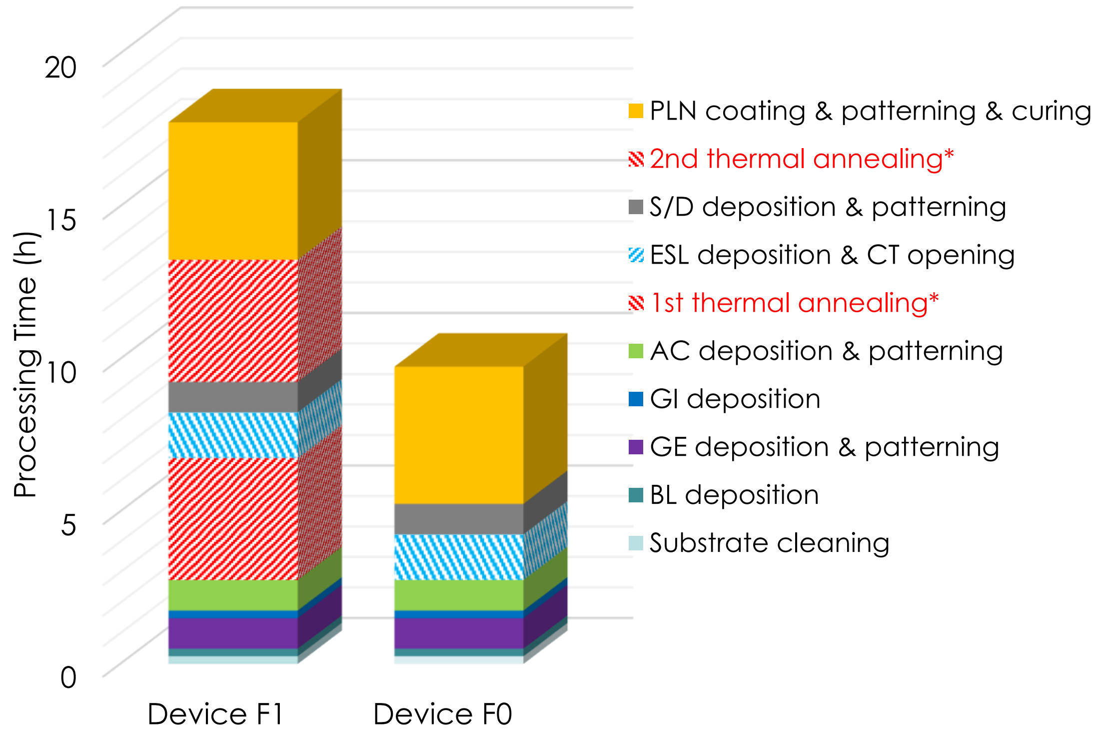
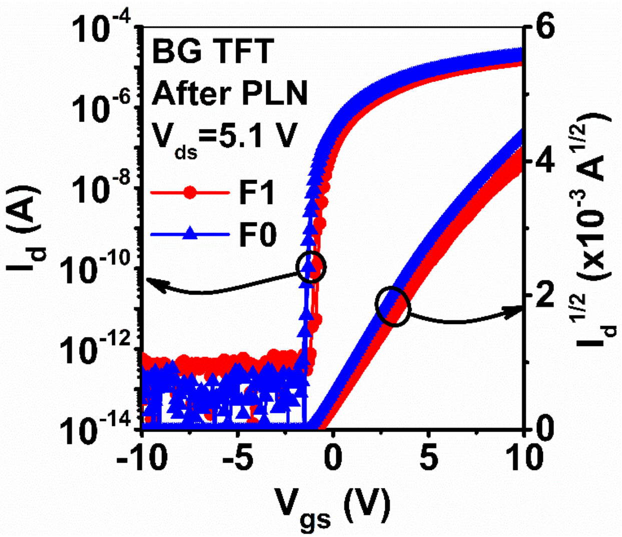
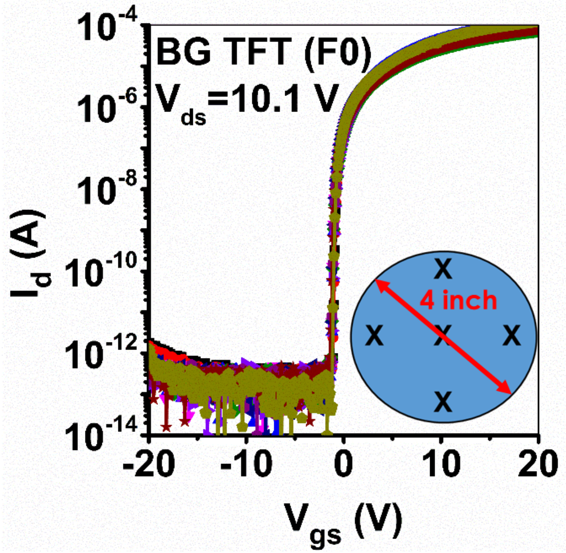
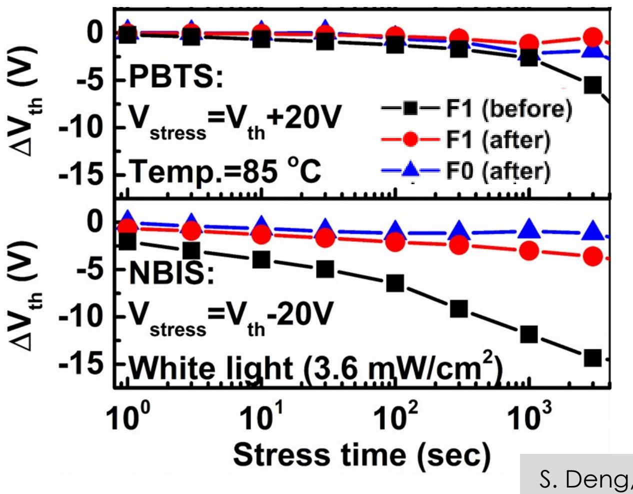
ESL hp-ITZO TFTs (II)









Key electrical parameters of Devices F1 and F0

	Device F1	Device F0
μ_{sat} (cm^2/Vs)	12.8	22.3
V_{th} (V)	-0.7	-0.8
On-off ratio	4.1×10^{9}	1.5×10^{10}
SS (mV/decade)	80.8	81.6

✓ No performance/uniformity/stability degradation in Device F0 despite the elimination of additional thermal annealing

→ A shorter production cycle and a lower thermal budget for cost-effective manufacturing.

S. Deng, et al. *J. Soc. Info. Disp.* 29, 318-327, 2021.
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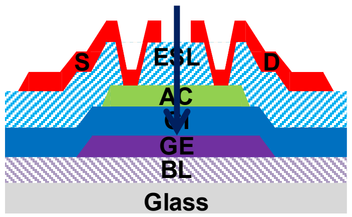
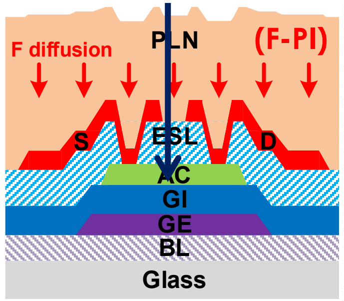
ESL hp-ITZO TFTs (III)

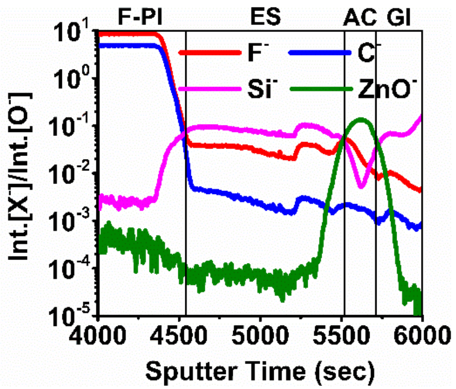
- **TOF-SIMS analysis in Device F0**

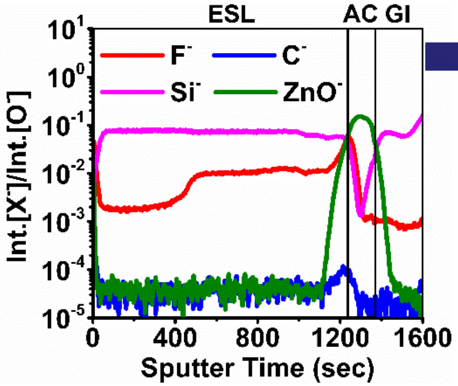


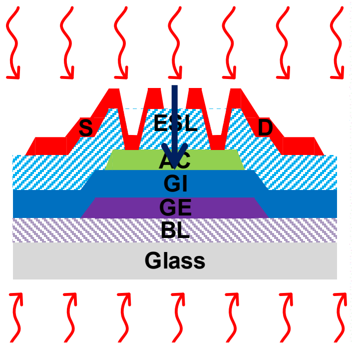
Device F0 before PLN



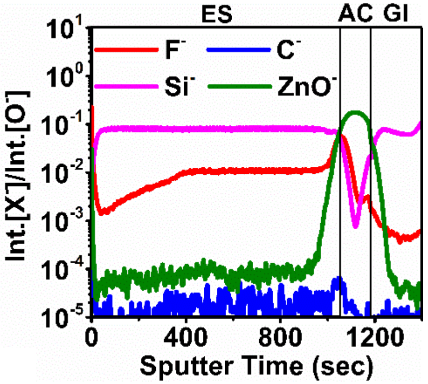
Device F0 after PLN



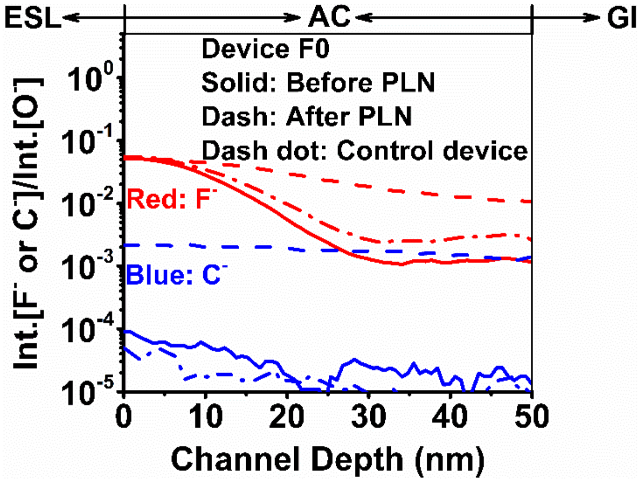




Control device F0*



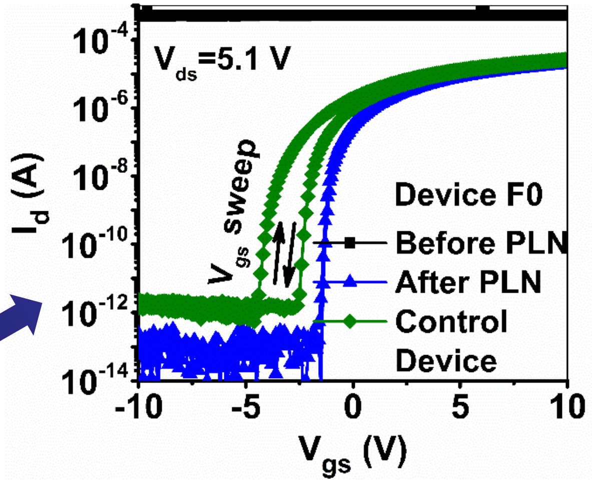
Similar F^- & C^- profiles



Diffusion of fragments like CF_x radicals from the F-PI PLN through the ESL into the AC

Oxygen deficiency passivation by F species

Improved performance



S. Deng, et al. *J. Soc. Info. Disp.* 29, 318-327, 2021.
Distinguished Paper Award, SID DW'2021.

Part 3: Practical Applications

AMOLED Prototype Display

Device → **Pixel** → **Panel**

Device

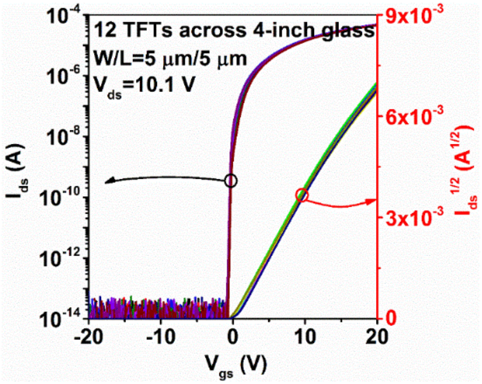
- TFT: TG-BC hp-ITZO
- Cs: double-layer cap.
- OLED: top emission

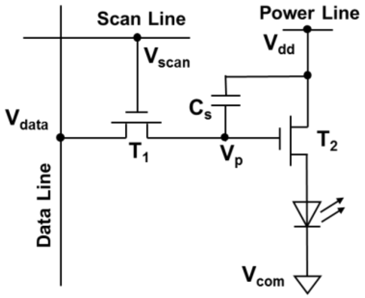
Pixel

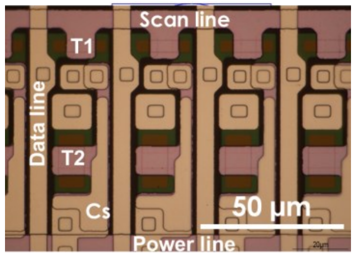
- Pixel circuit: 2T1C
- Pixel density: 287 ppi
- Resolution: 200(H) x 600(V)

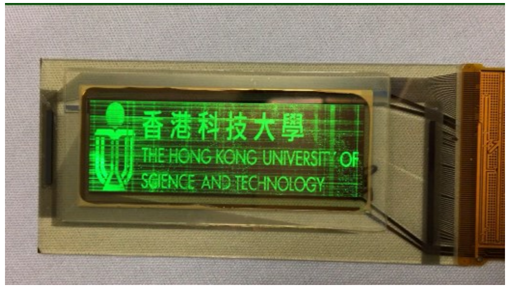
Panel

- Panel size: 2.2 in.
- Frame rate: 60 Hz
- Chip Assembly: COG
- AR: 40.7%









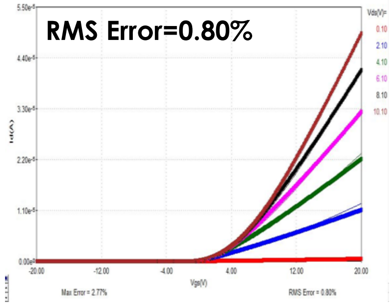
✓ By following the simplified process flow, the hp-ITZO TFT technology is applicable to low-cost AM-FPDs.

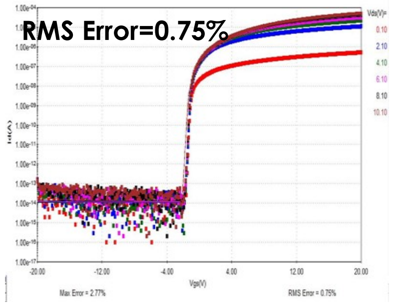
S. Deng, et al. *J. Soc. Info. Disp.* 29, 318-327, 2021.

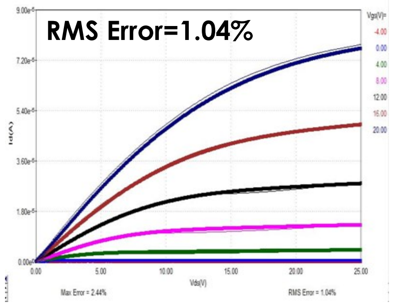
Integrated Circuits (I)

TFT modeling

- RPI-pTFT model
- BSIMProPlus

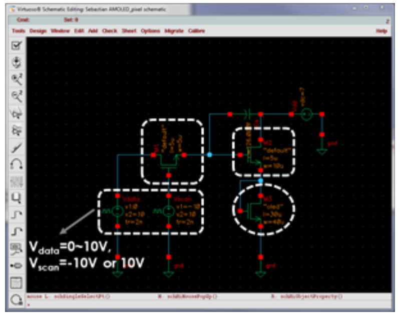






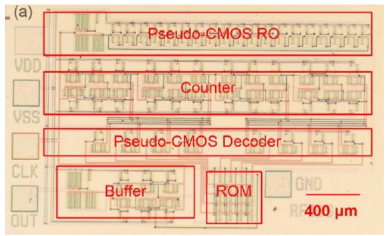
Circuit design & simulation

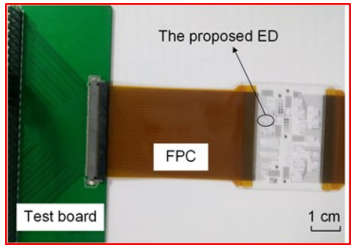
- Cadence ADE
- Synopsys Hspice
- … …



Tape-out

- HKUST-NFF
- … …

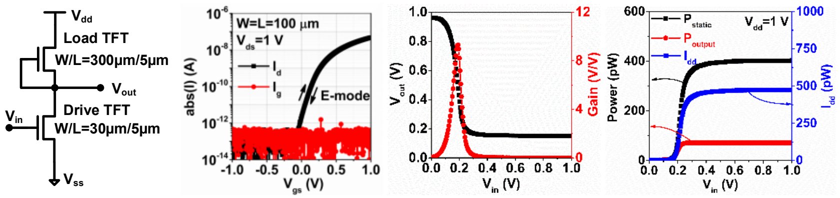




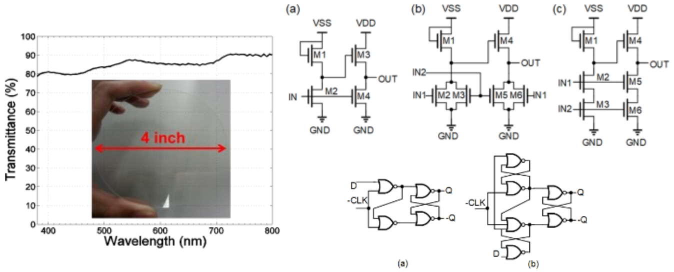
*Cooperation with SCUT

Integrated Circuits (II)

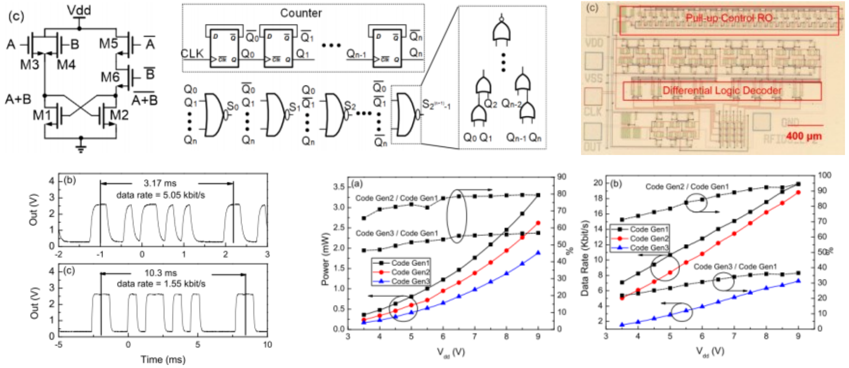
- **1-volt zero-V_{gs} inverter[1]** (power-delay product≈0.35 pJ)

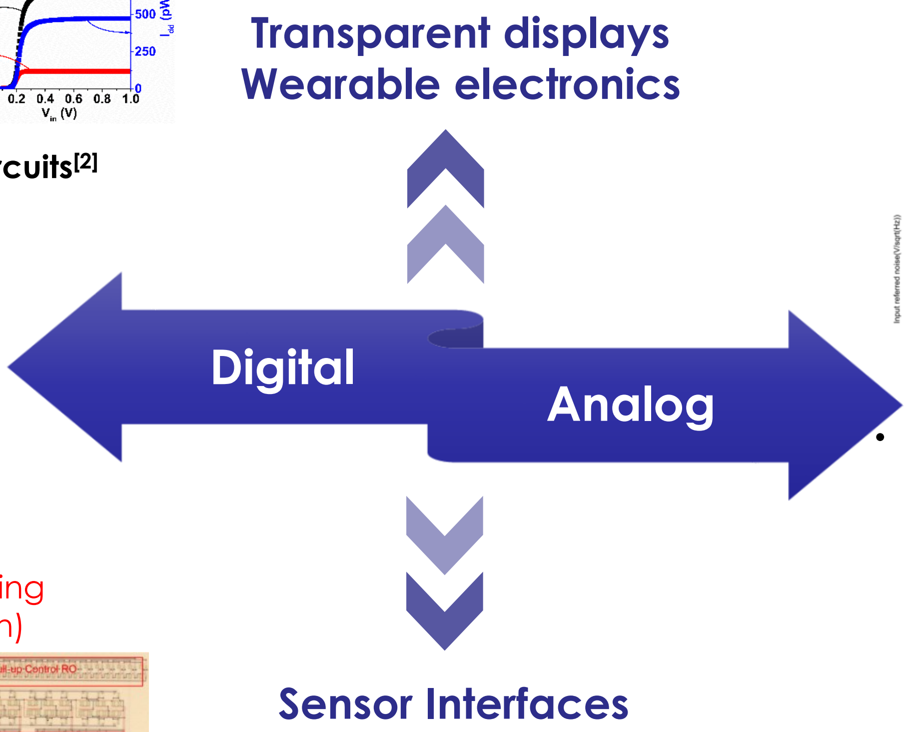


- **Fully transparent pseudo-CMOS digital circuits[2]** (T=77~92%, f_{osc}=42 kHz)

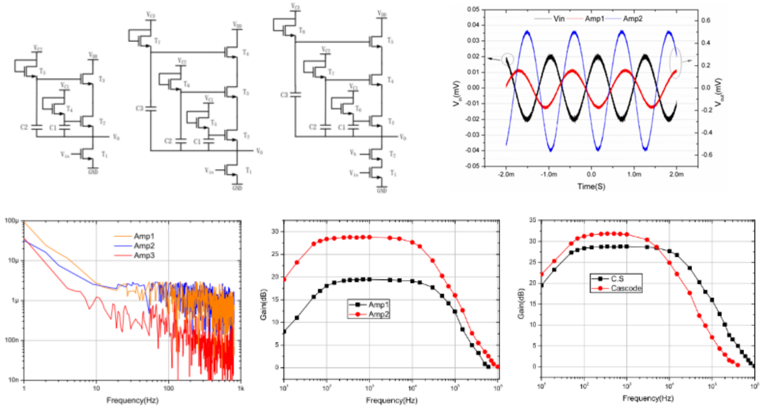


- **Low-power differential logic decoder[3]** (ISO/IEC15693 standard, ~40% power saving compared with the pseudo-CMOS design)

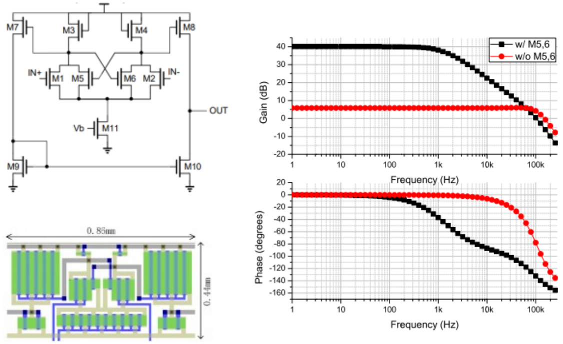




- **Capacitor-booststrap amplifier[4]** (Gain=32 dB, noise=38.3 μV_{rms} @ 200 Hz)



- **Negative-load amplifier** (Gain=40 dB, GBW=135 kHz, area=0.028 mm^2, power=0.226 mW)



[1] S. Deng, et al. *ICDT* 2021.
[2] Y. Xu, et al. *IEEE Trans. Electron Devices*, 65(12), 5395-5399, 2018.
[3] Y. Qin, et al. *IEEE Trans. Electron Devices*, 66(11), 4768-4773, 2019.
[4] H. Fan, et al. *IEEE Trans. Electron Devices*, 67(12), 5537-5543, 2020.

Conclusion

- Multicomponent hp-MO thin films have been developed by modifying both element composition and crystal morphology. Their electron mobility can surpass the upper limit in the amorphous counterparts.
- The hp-MO channels are applicable to high-performance TFTs with various structures. The cost-effective SA and ESL hp-ITZO TFTs have been demonstrated through device and processing innovations.
- The hp-MO TFT technology can support the implementation of energy-efficient, fully transparent electronics applications.

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  Prof. Dongxiang Luo (SCNU)
  Prof. Yuan LIU (GDUT)
  Dr. Wei ZHONG (GDUT)

- **Prof. Jun ZHOU & Jun's group (HUST)**

- **Facility platforms**

  納米系統製造實驗所 NANOSYSTEM FABRICATION FACILITY

  材料表徵與製備中心 (清水灣) Materials Characterization & Preparation Facility (CWB)

- **Funders**

  国家自然科学基金委员会 NSFC

  創新科技署 Innovation and Technology Commission

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Thank you for your kind attention!

Sunbin Deng

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先進顯示與光電子技術
國家重點實驗室
State Key Laboratory of Advanced Displays and Optoelectronics Technologies

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